WHAT IS CLAIMED IS:

1. A deframer for a wireless communication device, comprising:

an input interface unit operative to receive data to be deframed;

a detection unit operative to evaluate each data byte from the input interface unit to detect for bytes of specific values;

a state control unit operative to provide a first set of control signals indicative of specific tasks to be performed for deframing based in part on the detected bytes of specific values; and

a conversion unit operative to deframe the received data based on the first set of control signals and in accordance with a particular deframing scheme to provide deframed data.

2. The deframer of claim 1, wherein the data to be deframed conforms to a frame format defined by RFC1662.

3. The deframer of claim 1, wherein the input interface unit is operative to receive the data to be deframed in word of multiple bytes and, for each received word, provide one data byte at a time for evaluation by the detection unit.

4. The deframer of claim 1, wherein the detection unit is operative to detect for flag and escape bytes in the received data.

5. The deframer of claim 4, wherein the conversion unit is operative to remove flag and escape bytes in the received data.

6. The deframer of claim 5, wherein the conversion unit is further operative to un-escape a data byte following each detected escape byte in the received data.

7. The deframer of claim 4, wherein the conversion unit is further operative to provide a header word for each detected flag byte in the received data.

8. The deframer of claim 1, wherein the conversion unit is operative to check each deframed packet based on a frame check sequence (FCS) value associated with the packet.

9. The deframer of claim 1, further comprising:

an output interface unit operative to provide a second set of control signals for storing the deframed data to an output buffer.

10. The deframer of claim 9, wherein the output interface unit is further operative to perform byte alignment of the deframed data provided by the deframer.

11. The deframer of claim 1, wherein the deframer is operative to provide the deframed data in words of multiple bytes.

12. The deframer of claim 1, wherein the deframer is operative to deframe a block of data for each deframing operation.

13. The deframer of claim 12, wherein the data block corresponds to a Radio Link Protocol (RLP) packet.

14. The deframer of claim 12, further comprising:

a first register operative to store a value indicative of the number of deframed packets for the data block.

15. The deframer of claim 12, wherein the conversion unit is further operative to provide a first header for the start of the data block.

16. The deframer of claim 1, wherein the deframer is in one of a plurality of operating states at any given moment, and wherein the operating states include an idle state indicative of no deframing being performed and a process state indicative of deframing being performed.

17. The deframer of claim 16, wherein the operating states include an escape state indicative of processing for an escape byte and a header state indicative of generation of a header for the deframed data.

18. A deframer for a wireless communication device, comprising:

an input interface unit operative to receive an RLP packet of data to be deframed, one word at a time, and for each received word provide one data byte at a time for subsequent processing, and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC1662;

a detection unit operative to evaluate each data byte from the input interface unit to detect for flag, escape, and invalid bytes;

a conversion unit operative to process each data byte from the interface unit by removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and

an output interface unit operative to provide deframed data.

19. An integrated circuit for a wireless communication device, comprising:

an input interface unit operative to receive an RLP packet of data to be deframed, one word at a time, and for each received word provide one data byte at a time for subsequent processing, and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC1662;

a detection unit operative to evaluate each data byte from the input interface unit to detect for flag, escape, and invalid bytes;

a conversion unit operative to process each data byte from the interface unit by removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and

an output interface unit operative to provide deframed data.

20. A method of deframing an RLP packet of data comprising one or more PPP packets having a format defined by RFC1662, the method comprising:

receiving the RLP packet, one word at a time;

evaluating each byte of each received word to detect for flag and escape bytes;

providing status signals indicative of each detected flag and escape byte;

removing the flag and escape bytes;

un-escaping a data byte following each detected escape byte;

checking each PPP packet based on an FCS value associated with the packet; and

providing deframed data.

21. A framer for a wireless communication device, comprising:

an input interface unit operative to receive data to be framed;

a detection unit operative to evaluate each data byte from the input interface unit to detect for bytes of specific values;

a state control unit operative to provide a first set of control signals indicative of specific tasks to be performed for framing based in part on the detected bytes of specific values; and

a conversion unit operative to frame the received data based on the first set of control signals and in accordance with a particular framing scheme to provide framed data.

22. The framer of claim 21, wherein the framed data conforms to a frame format defined by RFC1662.

23. The framer of claim 21, wherein the input interface unit is operative to receive the data to be framed in word of multiple bytes and, for each received word, provide one data byte at a time for evaluation by the detection unit.

24. The framer of claim 21, wherein the conversion unit is further operative to insert a flag byte in response to receiving a first command.

25. The framer of claim 21, wherein the conversion unit is further operative to insert a frame check sequence (FCS) value in response to receiving a second command.

26. The framer of claim 21, wherein the conversion unit is operative to insert an escape byte upon detection of a data byte having one of the specific values.

27. The framer of claim 21, further comprising:

an output interface unit operative to provide a second set of control signals for storing the framed data to an output buffer.

28. The framer of claim 27, wherein the output interface unit is further operative to perform byte alignment of the framed data.

29. The framer of claim 27, wherein the output interface unit is operative to provide the framed data in words of multiple bytes.

30. The framer of claim 21, wherein the framer is operative to frame a block of data for each framing operation.

31. The framer of claim 30, wherein the data block corresponds to a Radio Link Protocol (RLP) packet.

32. The framer of claim 21, wherein the framer is in one of a plurality of operating states at any given moment, and wherein the operating states include an idle state indicative of no framing being performed and a process state indicative of framing being performed.

33. The framer of claim 32, wherein the operating states further include an escape state indicative of processing for an escape byte.

34. The framer of claim 32, wherein the operating states further include a flag state indicative of insertion of a flag byte for a framed packet and an FCS state indicative of insertion of an FCS value for the framed packet.

35. The framer of claim 21, further comprising:

a first register operative to store a value indicative of the number of framed packets for the data block.

36. A framer for a wireless communication device, comprising:

an input interface unit operative to receive a packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing;

a detection unit operative to evaluate each data byte from the input interface unit to detect for bytes of specific values;

a conversion unit operative to process each data byte from the interface unit to frame the received data by inserting an escaped byte for each data byte to be escaped and escaping the data byte, inserting a flag byte in response to receiving a first command, and inserting an FCS value in response to receiving a second command; and

an output interface unit operative to provide framed data having a format defined by RFC1662.

37. An integrated circuit for a wireless communication device, comprising:

an input interface unit operative to receive a packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing;

a detection unit operative to evaluate each data byte from the input interface unit to detect for bytes of specific values;

a conversion unit operative to process each data byte from the interface unit to frame the received data by inserting an escaped byte for each data byte to be escaped and escaping the data byte, inserting a flag byte in response to receiving a first command, and inserting an FCS value in response to receiving a second command; and

an output interface unit operative to provide framed data having a format defined by RFC1662.

38. A method of framing a packet of data to provide framed data having a format defined by RFC1662, comprising:

receiving the packet of data, one word at a time;

evaluating each data byte of each received word to detect for bytes to be escaped;

providing a status signal indicative of each data byte to be escaped;

inserting an escape byte for each data byte to be escaped and escaping the data byte;

inserting a flag byte in response to receiving a flag insert command;

inserting an FCS value in response to receiving an FCS insert command; and

providing framed data having the format defined by RFC1662.

39. An HDLC accelerator for a wireless communication device, comprising:

a deframer operative to receive a first block of data to be deframed, detect for data bytes of a first set of specific values, deframe the first data block in accordance with a particular deframing scheme, and provide deframed data for the first data block; and

a framer operative to receive a second block of data to be framed, detect for data bytes of a second set of specific values, frame the second data block in accordance with a particular framing scheme, and provide framed data for the second data block.

40. The HDLC accelerator of claim 39, wherein the data to be deframed in the first data block and the framed data for the second data block each have a format defined by RFC1662.

41. The HDLC accelerator of claim 39, further comprising:

at least one frame check sequence (FCS) generator operative to generate an FCS value for each packet to be framed or deframed.

42. The HDLC accelerator of claim 39, further comprising:

a first buffer operative to store the deframed data from the deframer.

43. The HDLC accelerator of claim 42, further comprising:

a second buffer operative to store the framed data from the framer.

44. The HDLC accelerator of claim 43, further comprising:

at least one buffer interface unit operable to retrieve the deframed data stored in the first buffer or the framed data stored in the second buffer.

45. The HDLC accelerator of claim 39, wherein the deframer and framer are each operated in one of a plurality of possible operating states.

46. A wireless communication device comprising:

a deframer operative to receive a first block of data to be deframed, detect for data bytes of a first set of specific values, deframe the first data block in accordance with a particular deframing scheme, and provide deframed data for the first data block;

a framer operative to receive a second block of data to be framed, detect for data bytes of a second set of specific values, frame the second data block in accordance with a particular framing scheme, and provide framed data for the second data block; and

a controller operative to direct deframing and framing by the deframer and framer, respectively.

47. The device of claim 46, further comprising:

a first buffer operative to store the deframed data from the deframer; and

a second buffer operative to store the framed data from the framer.

48. A multi-bit CRC generator, comprising:

a latch operative to store an N-bit value; and

a plurality of (M) 1-bit CRC generators coupled in series and in a loop with the latch, wherein each 1-bit CRC generator is operative to receive an N-bit value from a preceding 1-bit CRC generator or the latch and a respective input data bit, scale N-1 least significant bits (LSBs) of the received N-bit value by two, selectively add the scaled value with a predetermined value corresponding to a polynomial being implemented, and provide the selectively added result as an N-bit output for the1-bit CRC generator.

49. The multi-bit CRC generator of claim 48, wherein M is eight.

50. The multi-bit CRC generator of claim 48, wherein N is 16.

51. The multi-bit CRC generator of claim 48, wherein each 1-bit CRC generator includes

a first adder operative to add a most significant bit (MSB) of the received N-bit value with the input data bit to provide a control value,

a second adder operative to add the scaled value with the predetermined value to provide a summed value, and

a multiplexer operative to provide the scaled value if the control value is zero and the summed value if the control value is one, wherein the multiplexer output is the N-bit output for the 1-bit CRC generator.

52. The multi-bit CRC generator of claim 48, wherein each 1-bit CRC generator includes

a first adder operative to add a most significant bit (MSB) of the received N-bit value with the input data bit to provide a control value,

a gate operative to provide the predetermined value if the control value is one and a zero if the control value is zero, and

a second adder operative to add the scaled value with an output value from the gate to provide the N-bit output for the 1-bit CRC generator.